What is claimed is:

1. A compound semiconductor device comprising:

a substrate formed of a first compound semiconductor;

a graded channel layer formed on the substrate, and formed of a second compound semiconductor layer of which an energy band gap is made narrower inside than both ends by positioning a peak of a distribution of one constituent element into the inside and by continuously changing a ratio of the one constituent element in a thickness direction, and dosed with an impurity;

a barrier layer formed on the graded channel layer;

a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer; and

a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer.

2. A compound semiconductor device according to claim 1, wherein the second compound semiconductor layer is composed of a material that one constituent element is added in the first compound semiconductor, and the one constituent element has a function which makes the energy band gap of the second compound semiconductor layer narrower than that of the first

compound semiconductor.

3. A compound semiconductor device according to claim 1, wherein a peak of the one constituent element in the graded channel layer is positioned at a center of a layer thickness of the graded channel layer, or positioned at a position that is deviated from the center.

4. A compound semiconductor device according to claim 1, wherein a peak of carrier density in the graded channel layer is positioned at a center of a layer thickness of the graded channel layer, or deviates from the center.

5. A compound semiconductor device according to claim 4, wherein a peak of carrier density in the graded channel layer sifts to the substrate side from a center of a layer thickness of the graded channel layer.

6. A compound semiconductor device according to claim 1, wherein contact layers are formed between the source electrode and the barrier layer and between the drain electrode and the barrier layer respectively.

7. A compound semiconductor device according to claim 1, wherein a buffer layer is formed between the substrate and the graded channel layer.

8. A compound semiconductor device according to claim 1, wherein the first compound semiconductor

constituting the substrate is GaAs, and the second compound semiconductor layer constituting the graded channel layer is an InGaAs, and the one constituent element contained in the second compound semiconductor layer is indium.

9. A compound semiconductor device according to claim 1, wherein the first compound semiconductor constituting the substrate is GaAs, and the second compound semiconductor layer constituting the graded channel layer is a GaAsSb or an InGaSb, and the one constituent element contained in the second compound semiconductor layer is indium or antimony.

10. A compound semiconductor device according to claim 1, wherein the first compound semiconductor constituting the substrate is InP, and the second compound semiconductor layer constituting the graded channel layer is an InAsP or a GaAsSb or an InPSb, and one constituent element contained in the second compound semiconductor layer is indium or antimony.

11. A compound semiconductor device according to claim 1, wherein the second compound semiconductor layer is consisted of a ternary or quaternary of group III-V semiconductor including at least one of gallium and indium as group III element and including at least one of arsenic, phosphorus, and antimony as group V element.